

Figure 1

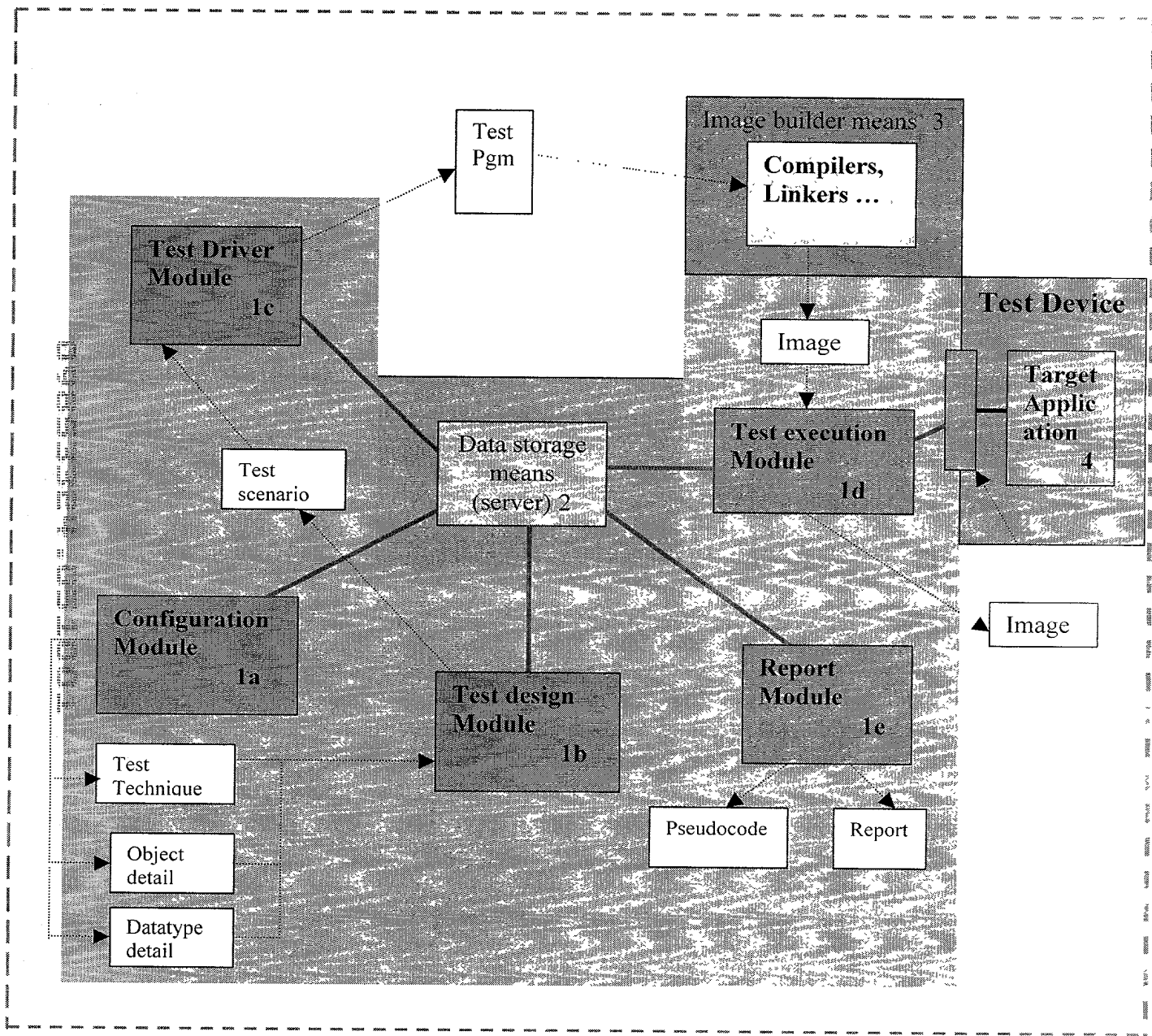


Figure 2

Figure 3 is a block diagram of a system architecture. The system includes a CPU, ROM, RAM, and various I/O devices connected to a central bus. The RAM is divided into three sections: Image Builder Means (3), Test generation means (1) (Client), and Data Storage Means (2) (Server). The system also includes a Display Device, Frame Memory, Input Device, External Storage, and Communication I/F. The Communication I/F is connected to a To Communication network (5), which is further connected to a Firewall (FW) and a Target Application (4). A Test Device is connected to the Target Application (4).

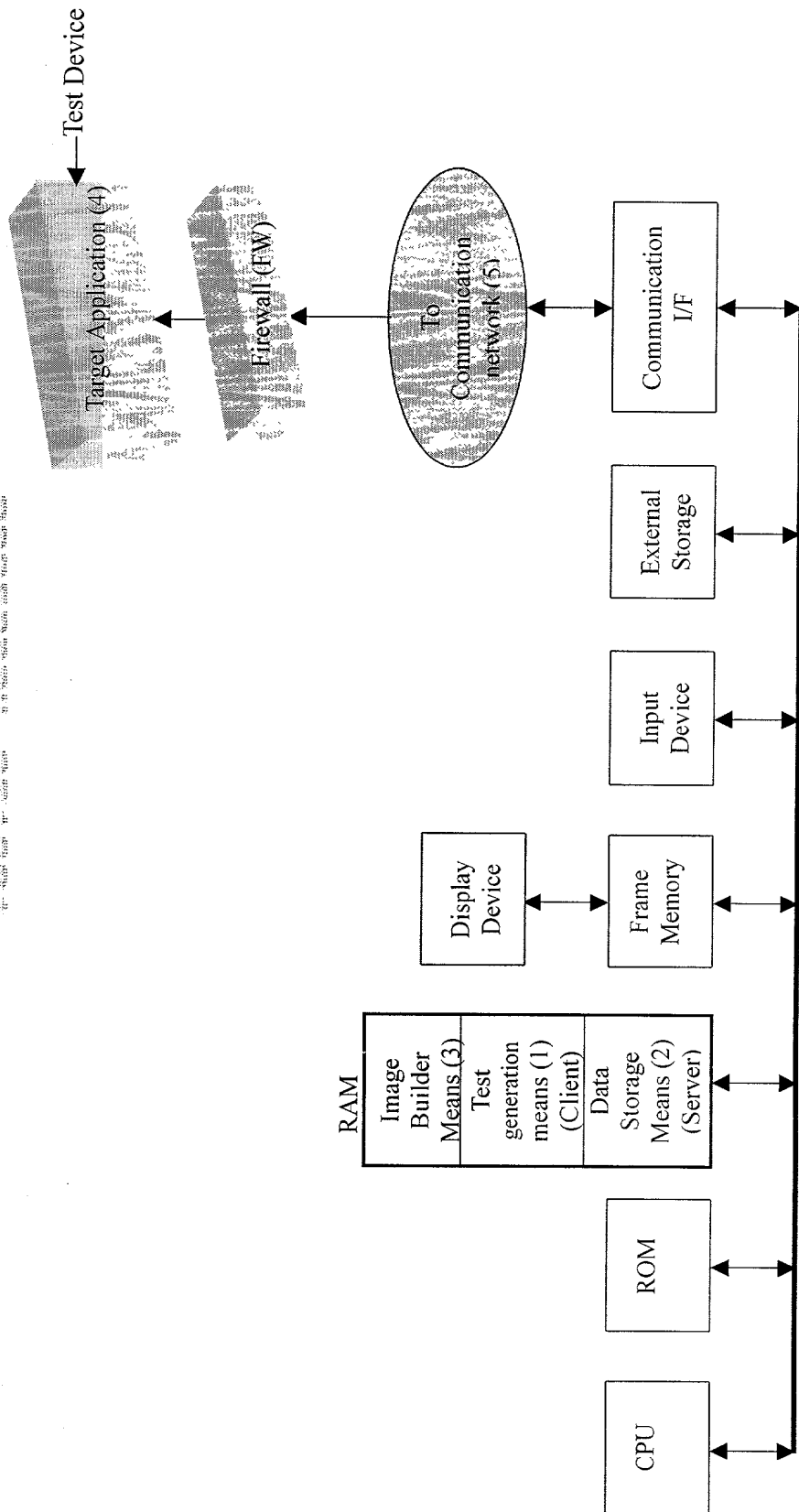


Figure 3

Figure 4 is a block diagram of a test system architecture. The diagram shows a central 'Communication Network (5)' connected to three main components: a 'Test generation means (1) (Client)', a 'Target Application (4)', and a 'Test Device'. The 'Test generation means (1) (Client)' is connected to a 'Communication I/F' and a 'Firewall (FW)'. The 'Target Application (4)' is connected to the 'Firewall (FW)'. The 'Test Device' is connected to the 'Target Application (4)'. The 'Test generation means (1) (Client)' is further connected to a 'CPU', 'ROM', 'RAM', 'Data Storage Means (2) (Server)', 'Frame Memory', 'Input Device', 'External Storage', and 'Display Device'. The 'Test Device' is connected to a 'CPU', 'ROM', 'RAM', 'Image Builder Means (3)', 'Frame Memory', 'Input Device', 'External Storage', and 'Display Device'. The 'Communication Network (5)' is connected to the 'Communication I/F' and the 'Firewall (FW)'.

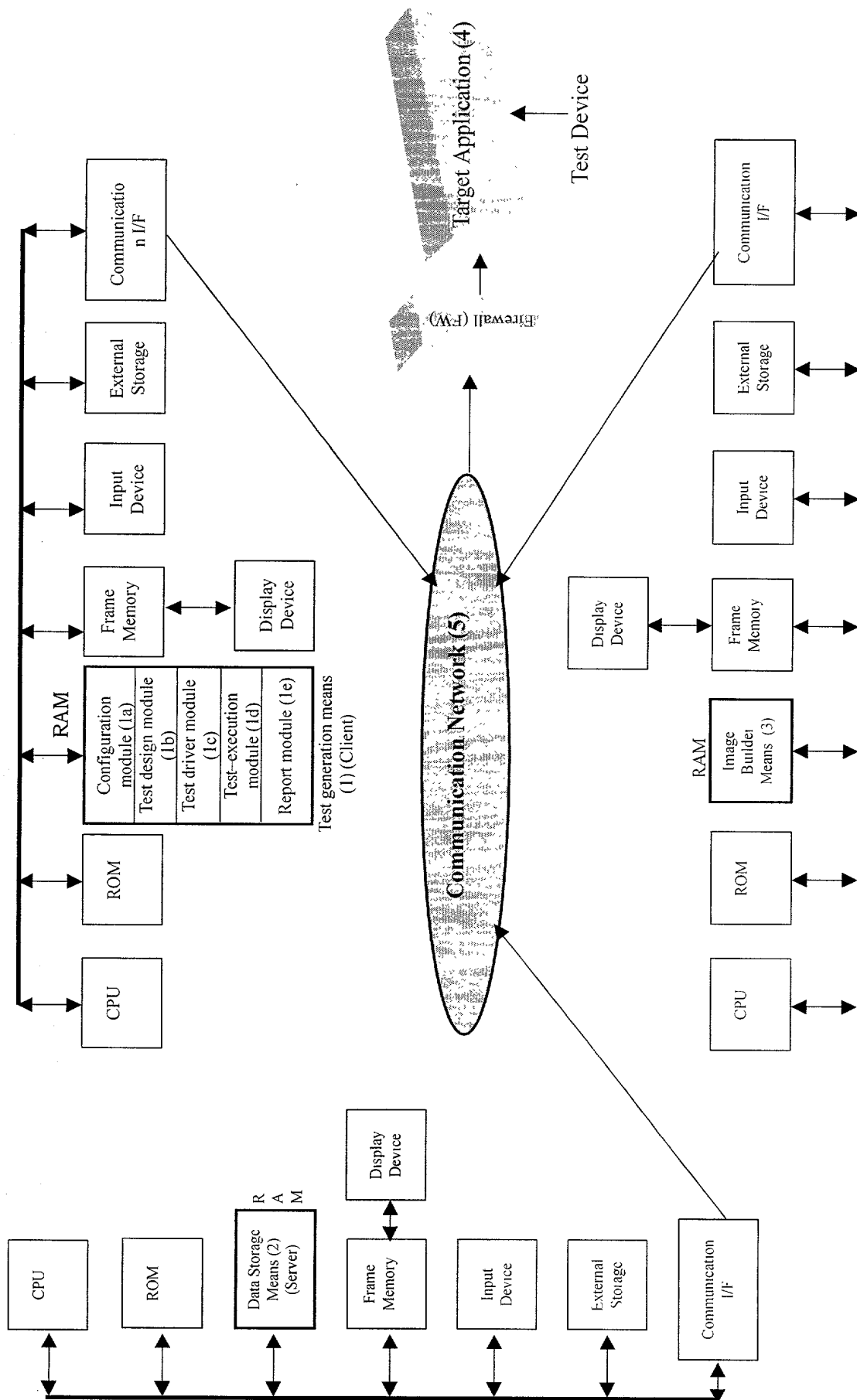


Figure 4

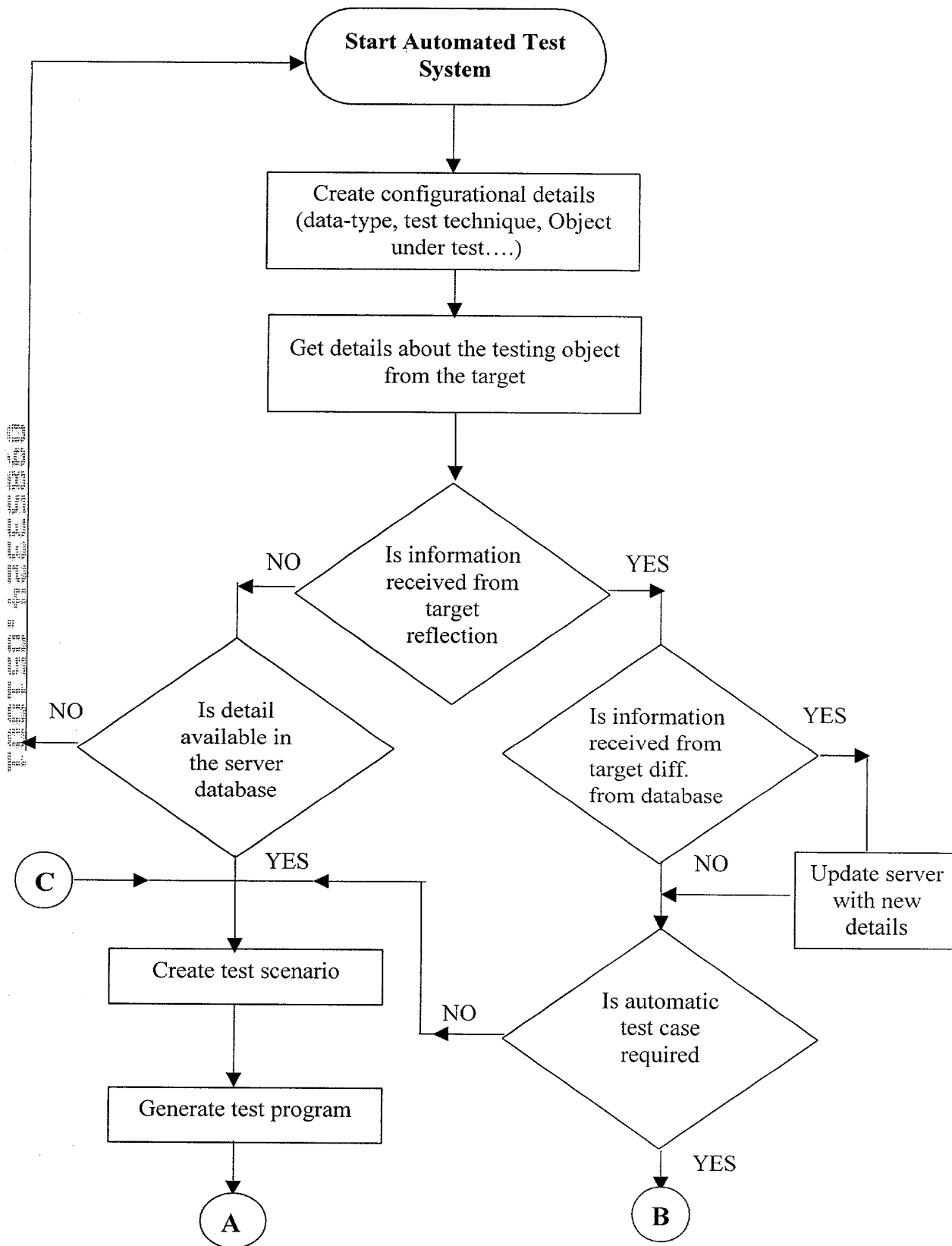


Figure 5a

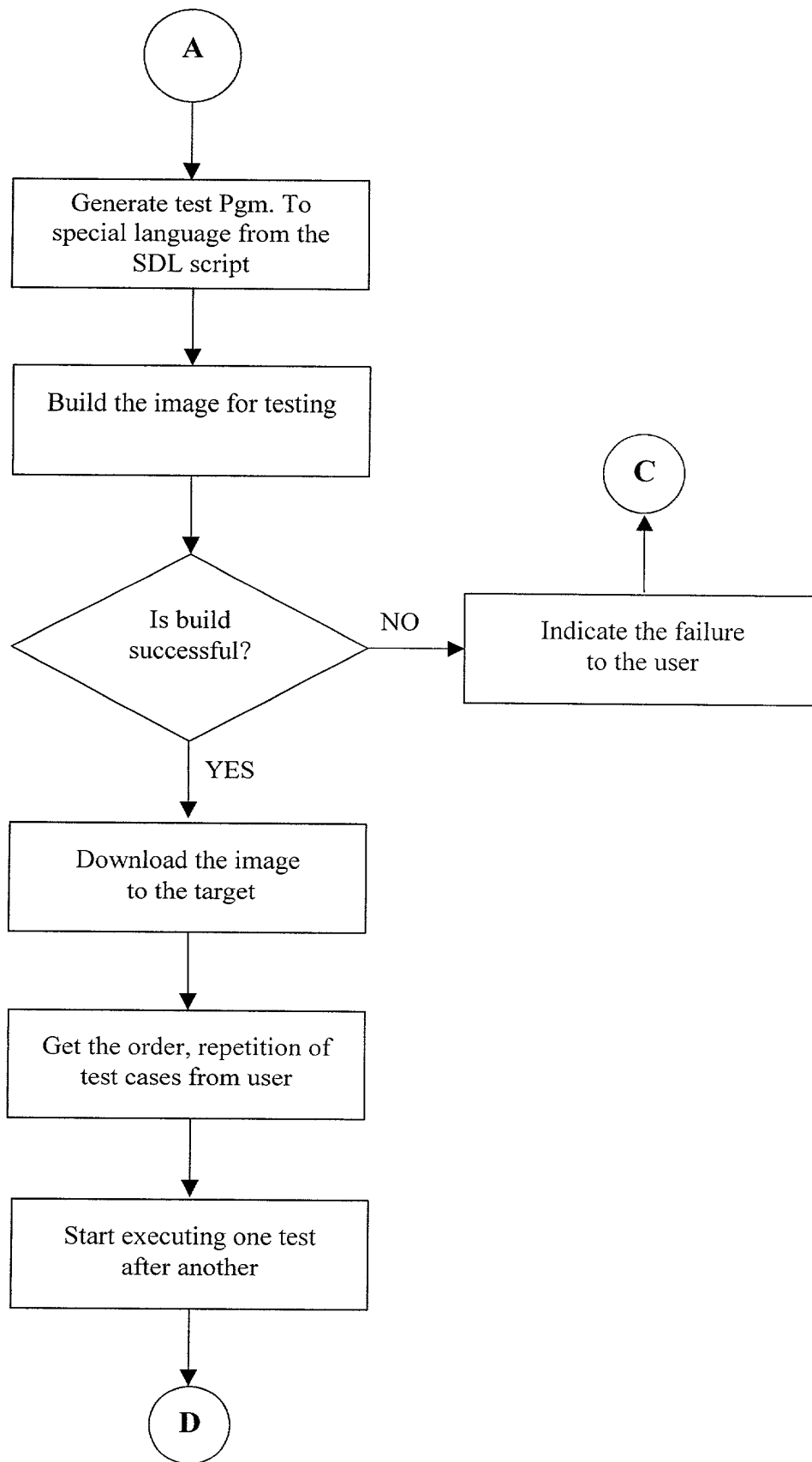


Figure 5b

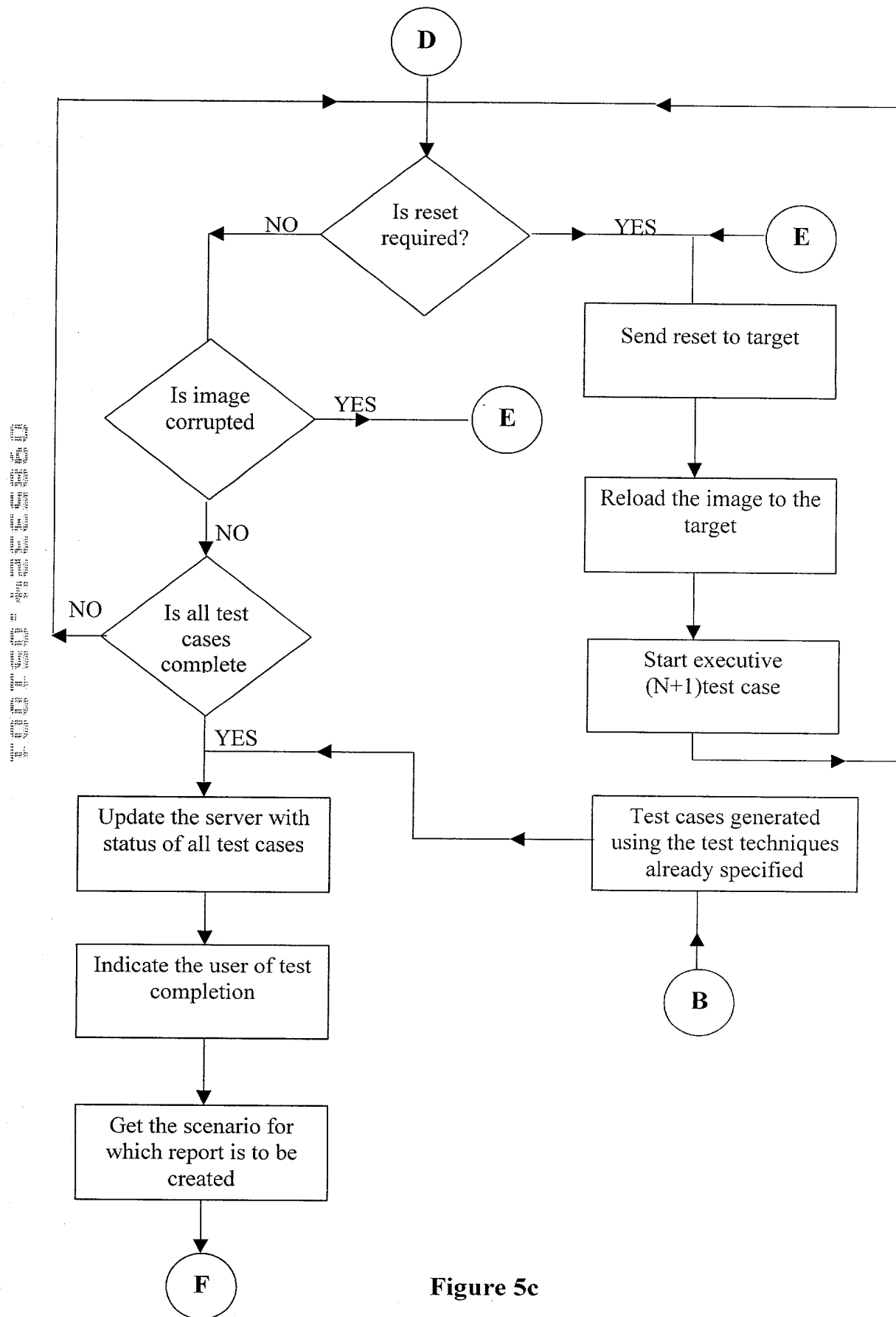


Figure 5c

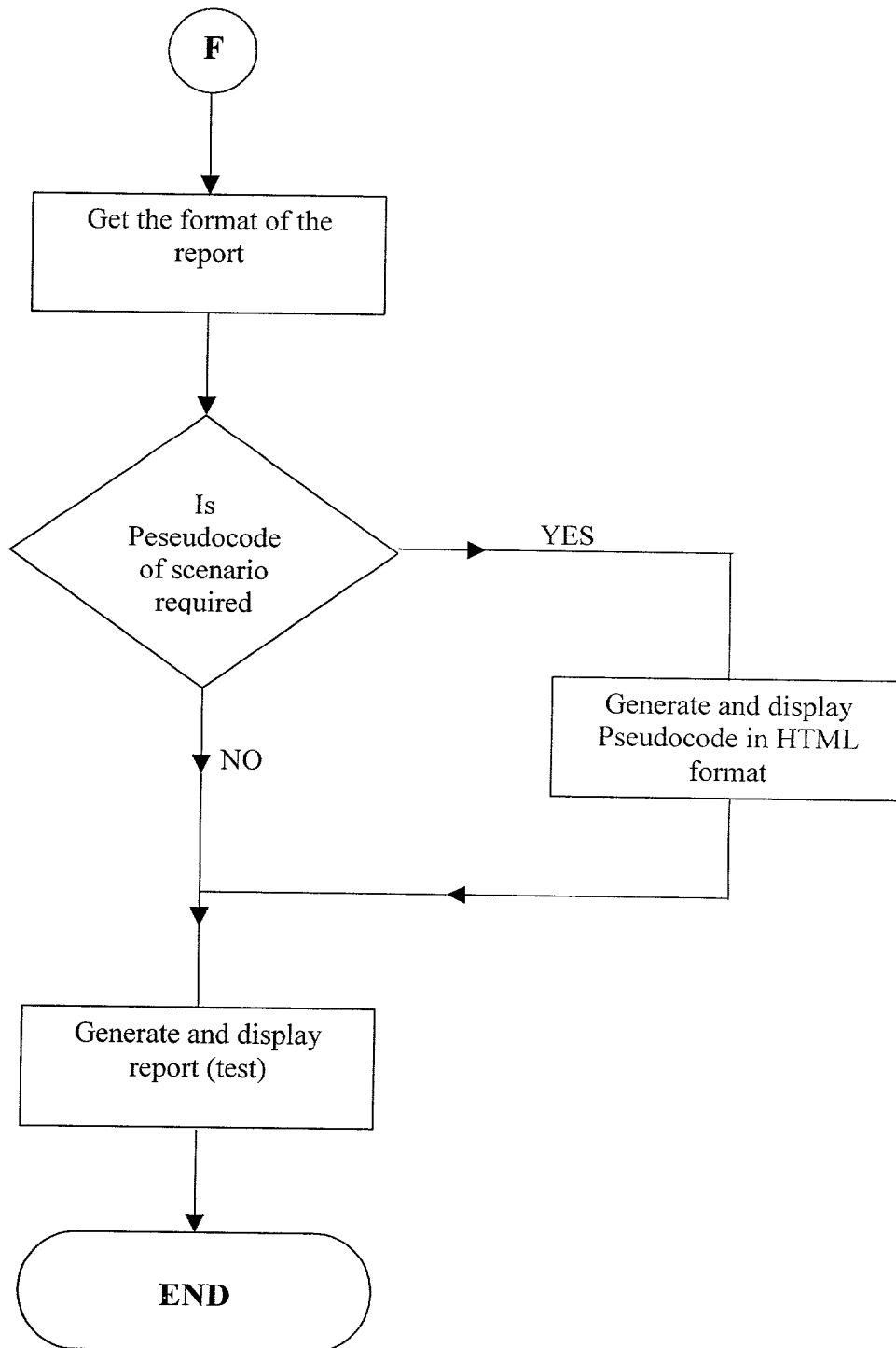


Figure 5d

TEST SCENARIO GENERATION

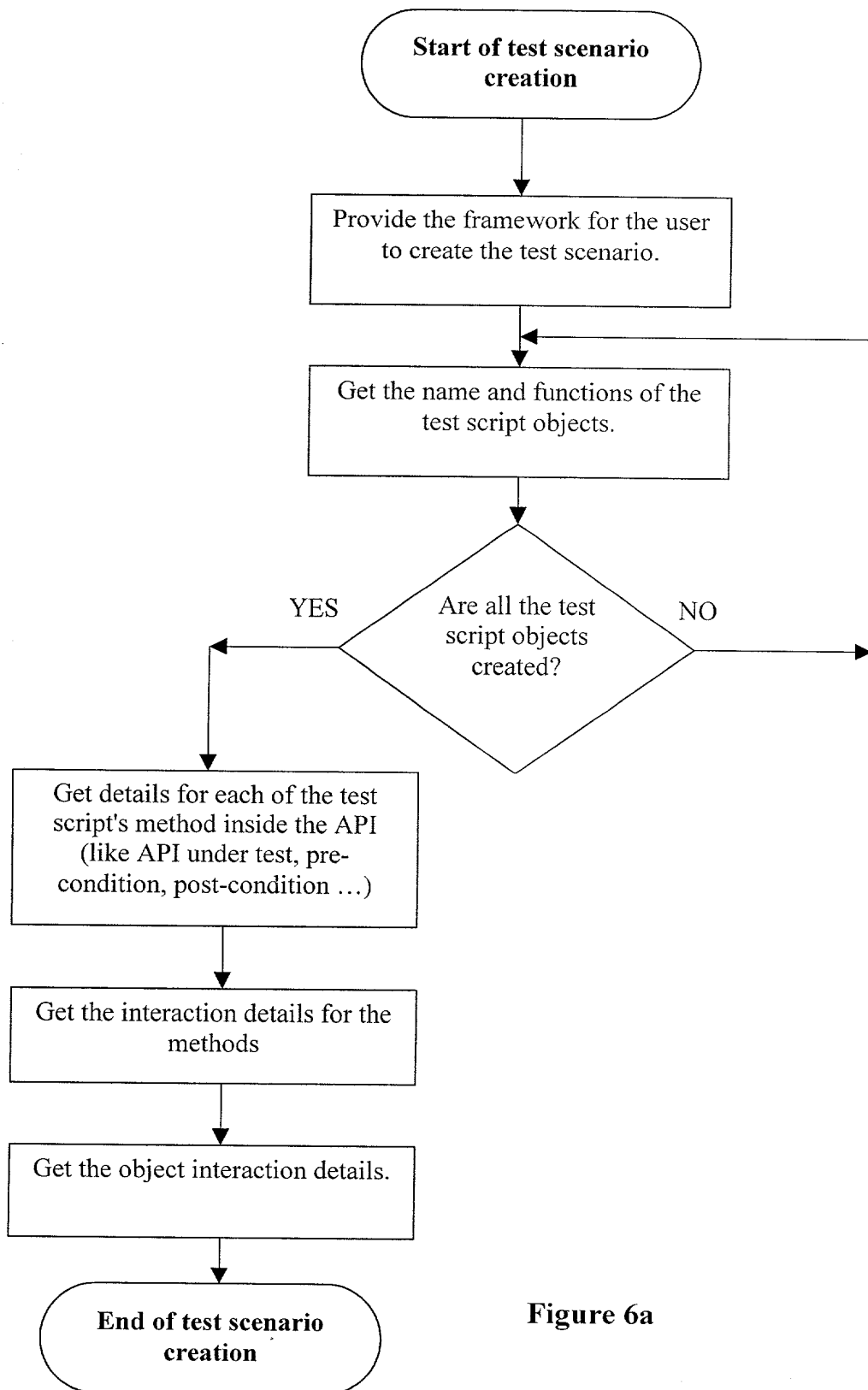


Figure 6a

TEST CASE GENERATION

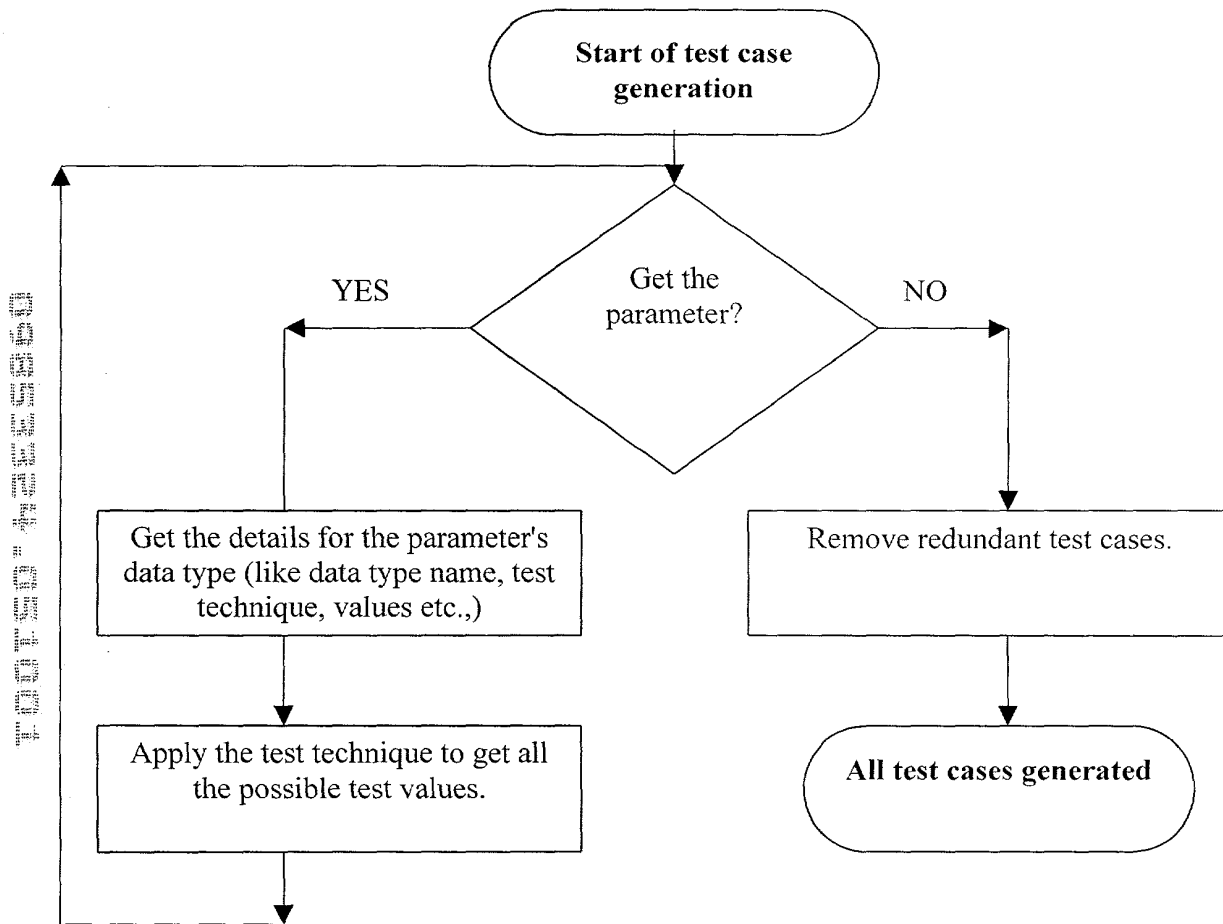


Figure 6b

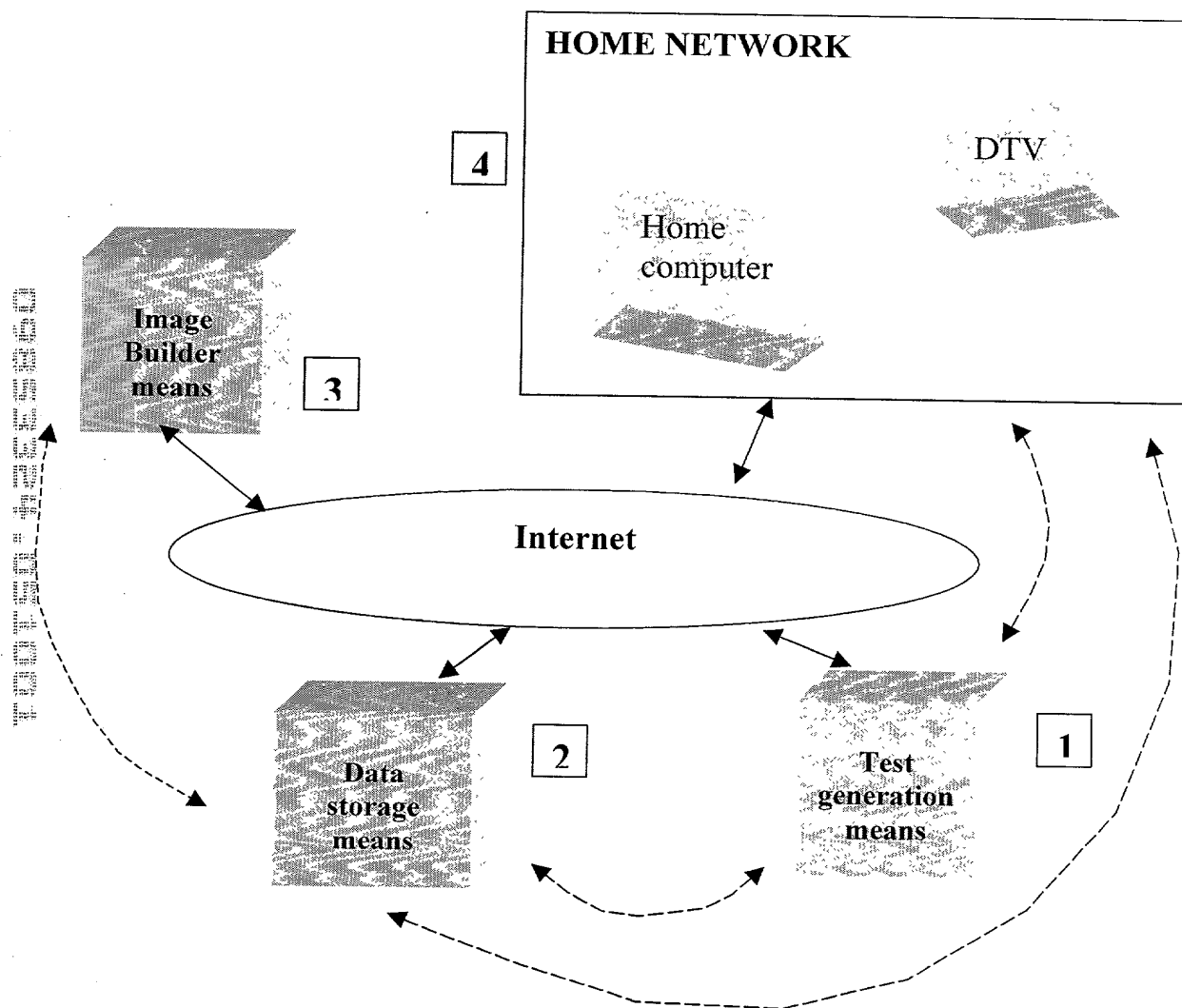


Figure 7